In the Specification:

Please replace paragraph **[0030]** with the following paragraph:

-- **[0030]** In the ~~example~~ illustrated example, when a processor 202 executes a memory operation, the request is passed to an L0 cache 302. Typically, the L0 cache 302 is internal to the processor 202. However, the L0 cache 302 may be external to the processor 202. If the L0 cache 302 holds the requested memory in a state that is compatible with the memory request (e.g., a write request is made and the L0 cache holds the memory in an "exclusive" state), the L0 cache 302 fulfills the memory request (i.e., an L0 cache hit). If the L0 cache 302 does not hold the requested memory (i.e., an L0 cache miss), the memory request is passed on to an L1 cache 204a which is typically external to the processor 202, but may be internal to the processor 202.--.

Please replace paragraph **[0038]** with the following paragraph:

-- **[0038]** A write-miss (WM) event is caused by the multi-processor module 106 attempting to write a cache line to a cache 204a when that cache 204a does not hold the cache line. A read-miss-exclusive (RME) event is caused by the multi-processor module 106 attempting to read a cache line from one cache 204a when that cache 204a does not hold the cache line, and no other cache 204 currently holds the cache line. A read-miss-shared (RMS) event is caused by the multi-processor module 106 attempting to read a cache

line from one cache 204a when that cache 204a does not hold the cache line, but another cache 204 does hold the cache line in the shared state. A read-hit (RH) event is caused by the multi-processor module 106 attempting to read a cache line from a ~~eache204a~~ cache 204a that holds the cache line. Other caches 204 holding the same line (but not supplying the line) see such a read as a snoop-hit-on-read (SHR) event. A write-hit (WH) event is caused by the multi-processor module 106 attempting to write a cache line to a cache 204a that holds the cache line. Other caches 204 holding the same line see such a write as a snoop-hit-on-write (SHW) event. A snoop hit associated with a read operation where there is an intent to modify the data is handled the same way as a snoop-hit-on-write (SHW) event.--.

Please replace paragraph **[0064]** with the following paragraph:

-- **[0064]** The illustrated process 700 begins by waiting for the internal inquiry (block 702). When the internal inquiry is received, the process 700 determines if the cache line associated with the internal inquiry is in the L1 cache 204a in the exclusive state 404 or the shared state 408 (block 704). If the cache line associated with the internal inquiry is in the L1 cache 204a in the exclusive state 404 or the shared state 408, the process 700 determines if the L2 cache 204b is inclusive of the L1 cache204a (block 706). If the L2 cache 204b is inclusive of the L1 ~~eache204a~~ cache 204a, the process 700 invalidates the cache line (block 708) and posts a ~HIT signal (i.e., a NO HIT or a MISS) signal from the L1 cache 204a (block 710). If the L2 cache 204b is not inclusive of the L1 ~~eache204a~~ cache 204a (block 706), the process

~~700posts~~ 700 posts a hit signal (block 712).~~--~~.